WHAT IS CLAIMED IS:

1. A method for forming a dual damascene structure for a semiconductor device comprising the steps of:

providing conductive regions on a first layer;

forming an interlevel dielectric layer over the first layer;

forming an etch stop layer over the interlevel dielectric layer, the etch stop layer including a polymer material having a dielectric constant of less than about 3.0;

patterning the etch stop layer to form a via pattern;

depositing a trench dielectric layer on the etch stop layer and in holes of the via pattern;

forming trenches in the trench dielectric layer by etching the trench layer in accordance with a trench pattern; and

forming vias in the interlevel dielectric layer by etching through the trenches using the etch stop layer to self-align the trenches to the vias and expose the conductive regions on the first layer.

2. The method as recited in claim 1, wherein the polymer includes at least one of polyorylene-ether and polybenzoxazole dielectric.

3. The method as recited in claim 1, wherein the step of providing conductive regions on a first layer includes providing one of metal lines and diffusion regions.

4. The method as recited in claim 1, further comprising the step of forming a cap layer on the conductive regions to protect the conductive regions from oxidation.

5. The method as recited in claim 1, wherein the interlevel dielectric layer and the trench dielectric layer are comprised of a same material.

6. The method as recited in claim 5, wherein the same material includes one of a nitride and an oxide.

7. The method as recited in claim 1, wherein the interlevel dielectric layer and the trench dielectric layer are selectively etchable relative to the etch stop layer.

8. The method as recited in claim 1, wherein the interlevel dielectric layer and the trench dielectric layer are comprised of a different material.

9. The method as recited in claim 1, wherein the step of patterning the etch stop layer to form a via pattern includes employing a hard mask layer to form the via pattern.

10. The method as recited in claim 1, further comprising the step of depositing conductive material to concurrently form contacts in the vias and conductive lines in the trenches.

11. The method as recited in claim 1, wherein the step of forming an etch stop layer over the interlevel dielectric layer includes spinning on and curing the polymer.

12. The method as recited in claim 1, wherein the etch stop layer includes a thickness of between about 100 nm to about 250 nm.

13. A method for forming a dual damascene structure for a semiconductor device comprising the steps of:

providing conductive regions on a first layer;

forming an interlevel dielectric layer over the first layer, the interlevel dielectric layer including a polymer material having a dielectric constant of less than about 3.0;

forming an etch stop layer over the interlevel dielectric layer;

patterning the etch stop layer to form a via pattern;

depositing a trench dielectric layer on the etch stop layer and in holes of the via pattern, the trench dielectric layer including a polymer material having a dielectric constant of less than about 3.0;

forming trenches in the trench dielectric layer by etching the trench layer in accordance with a trench pattern; and

forming vias in the interlevel dielectric layer by etching through the trenches using the etch stop layer to self-align the trenches to the vias and expose the conductive regions on the first layer.

14. The method as recited in claim 13, wherein the polymer includes at least one of polyorylene-ether and polybenzoxazole dielectric.

15. The method as recited in claim 13, wherein the step of providing conductive regions on a first layer includes providing one of metal lines and diffusion regions.

16. The method as recited in claim 13, further comprising the step of forming a cap layer on the conductive regions to protect the conductive regions from oxidation.

17. The method as recited in claim 13, wherein the etch stop layer includes one of an oxide and a nitride.

18. The method as recited in claim 13, wherein the interlevel dielectric layer and the trench dielectric layer are selectively etchable relative to the etch stop layer.

19. The method as recited in claim 13, wherein the interlevel dielectric layer and the trench dielectric layer are comprised of a different polymer material.

20. The method as recited in claim 13, wherein the step of forming trenches in the trench dielectric layer by etching the trench layer in accordance with a trench pattern includes the step of patterning the trench dielectric layer using an oxide layer as a hard mask.

21. The method as recited in claim 13, further comprising the step of depositing conductive material to concurrently form contacts in the vias and conductive lines in the trenches.

22. The method as recited in claim 13, wherein the step of forming an interlevel dielectric layer includes spinning on and curing the polymer.

23. The method as recited in claim 13, wherein the step of depositing a trench dielectric layer includes spinning on and curing the polymer.

24. A dual damascene structure comprising:

conductive regions on a first layer;

an interlevel dielectric layer formed over the first layer and having vias therethrough;

a trench dielectric layer having trenches formed therein in communication with the vias;

an etch stop layer formed between the interlevel dielectric layer and the trench dielectric layer;

the trenches and the vias being filled with a conductive material, the conductive material forming conductive lines in the trenches which are connected to the conductive regions of the first layer by contacts formed in the vias; and

at least one of the interlevel dielectric layer, the trench dielectric layer and the etch stop layer include a polymer material having a dielectric constant of less than or equal to 3.0.

25. The structure of claim 24, wherein the polymer includes at least one of polyorylene-ether and polybenzoxazole dielectric.

26. The structure of claim 24, wherein the interlevel dielectric layer and the trench dielectric layer include the polymer material.

27. The structure of claim 24, wherein the etch stop layer includes the polymer material.

28. The structure of claim 27, wherein the etch stop layer includes a thickness of between about 100 nm and about 250 nm.

29. The structure of claim 27, wherein adjacent conductive lines have a space of less than or equal to 0.25 microns therebetween.